Notice of Allowability	Application No.	Applicant(s)	
	10/705,765	RADICE ET AL.	
	Examiner	Art Unit	(h)
	Kimberly E. Glenn	2817	
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI	(OR REMAINS) CLOSED ir or other appropriate commu GHTS. This application is s	n this application. If not include unication will be mailed in due c	d course. <b>THIS</b>
1. This communication is responsive to <u>9/14/05</u> .			
2. X The allowed claim(s) is/are 1.3-9.11-17 and 19-21.			
<ul> <li>3.  Acknowledgment is made of a claim for foreign priority un a)  All b)  Some* c)  None of the: <ol> <li>1.  Certified copies of the priority documents have</li> <li>2.  Certified copies of the priority documents have</li> <li>3.  Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)).</li> </ol> </li> <li>* Certified copies not received:</li> </ul>	been received. been received in Application	n No	on from the
Applicant has THREE MONTHS FROM THE "MAILING DATE" of noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		a reply complying with the requ	uirements
4. A SUBSTITUTE OATH OR DECLARATION must be submi INFORMAL PATENT APPLICATION (PTO-152) which give			TICE OF
5. CORRECTED DRAWINGS ( as "replacement sheets") musi	t be submitted.		
(a) ☐ including changes required by the Notice of Draftsperso		v ( PTO-948) attached	
1) 🔲 hereto or 2) 🔲 to Paper No./Mail Date			
(b) ☐ including changes required by the attached Examiner's Paper No./Mail Date	: Amendment / Comment or	in the Office action of	
Identifying Indicia such as the application number (see 37 CFR 1. each sheet. Replacement sheet(s) should be labeled as such in th			back) of
<ol> <li>DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT F</li> </ol>	sit of BIOLOGICAL MATE	ERIAL must be submitted. N	ote the
Attachment(s)  1. ☐ Notice of References Cited (PTO-892)  2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)  3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/06 Paper No./Mail Date	6. ☐ Interview St Paper No./ 8), 7. ☐ Examiner's	formal Patent Application (PTO ummary (PTO-413), Mail Date Amendment/Comment Statement of Reasons for Allov	·

#### **DETAILED ACTION**

# Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 5, 9,11, 12, 14, 19 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuo US Patent 6,317,016.

Kuo disclose in figure 2b, a differential gyrator-based signal filter 200, for an LC ladder implementation. The gyrator-based signal-filter 200 includes a plurality of transconductance cells G1-G15, and a plurality of capacitors C1-C7 and CL2, CL4 and CL6. The plurality of transconductance cells are arranged to simulate the inductance ladder section and at least on subsequent inductance ladder section. The first and subsequent inductance ladder section has at least one associated capacitance value scaled to accommodate a feed forward and feedback path through the transconductance cells. The gyrator-based signal-filter 200 implements an LC ladder filter with three inductors represented by three gyrator-capacitor arrangements. The three gyrator-capacitor arrangements respectively correspond to the three LC ladder filter sections of FIG. 2a. For example, G3, G4, G5, G6 together with CL2 form an inductor. The differential outputs are connected to capacitors C7. (Column 5; line 26-47) With regards to claims 9, 11, 12, 14, figure 3 shows a transconductance cell with a common mode feedback connected to differential outputs for implementing the f

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disclosed filter circuit. The common mode feedback circuit 312 includes a high impedance circuit 360 and a signal sampling circuit 362. The high impedance circuit compares the sampled common mode voltage to a reference voltage and provides a common mode feedback to the transconductance cell 310. The transconductance cell includes MOS transistors.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuo US Patent 6,317,016 in view of Reed et al US Patent 6,614,609.

Kuo disclose in figure 2b, a differential gyrator-based signal filter 200, for an LC ladder implementation. The gyrator-based signal-filter 200 includes a plurality of transconductance cells G1-G15, and a plurality of capacitors C1-C7 and CL2, CL4 and CL6. The plurality of transconductance cells are arranged to simulate the inductance ladder section and at least on subsequent inductance ladder section. The first and subsequent inductance ladder section has at least one associated capacitance value scaled to accommodate a feed forward and feedback path through the transconductance cells. The gyrator-based signal-filter 200 implements an LC ladder filter with three inductors represented by three gyrator-capacitor arrangements. The three gyrator-capacitor arrangements respectively correspond to the three LC ladder

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filter sections of FIG. 2a. For example, G3, G4, G5, G6 together with CL2 form an inductor. The differential outputs are connected to capacitors C7. (Column 5; line 26-47)

Thus, Kuo is shown to teach all the limitation of the claim with the exception of a disk drive read channel signal line coupled to the circuit input to provide data stored on disk drive to the circuit.

Reed et al discloses in prior art figure 1, an example of the user data path for a disk drive system 100. Disk drive system 100 includes a disk device 102 and associated control circuitry 104. Disk device 102 includes storage media 106. Some examples of storage media 106 include magnetic disks and optical disks. Control circuitry 104 includes write channel 110 and read channel 120. Write channel 110 includes encoder 112, compensation 114, and write interface 116 connected in series. Read channel 120 includes sampler 121, adaptive filter 122, interpolator 123, detector 124, and decoder 125 connected in series. Interface 116 and sampler 121 are coupled to disk device 102.

It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiates the claimed apparatus from a prior art apparatus satisfy the claimed structural limitations.

### Allowable Subject Matter

Claims 1, 3, 4, 6, 7 and 8 are allowed.

Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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The following is a statement of reasons for the indication of allowable subject matter: With regards to claims 1, 3, 6, and 8, the prior art of record does not disclose or fairly teach a each integrator having a bipolar transistor input circuit and a MOS transistor bias circuit portion and having a least on output of the second integrate feedback connected to the bias circuit portion of the same integrator through a feedback block. With regards to claim 4, the prior art of record does not disclose or fairly teach the outputs of the first integrator being connected to the inputs of the second integrator and being coupled to ground by respective diodes. With regard to claim 7, the prior art of record does not disclose or fairly teach using the specific equation recited in claim 7 in order to emulate a capacitor.

#### **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly E. Glenn whose telephone number is (571)-272-1761. The examiner can normally be reached on Monday-Friday 7:30 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimberly E Glenn Examiner Art Unit 2817

keg

### **REASONS FOR ALLOWANCE**

The following is an examiner's statement of reasons for allowance: With regards to claims 1, 3, 6, 8, 19 and 20, the prior art of record does not disclose or fairly teach a each integrator having a bipolar transistor input circuit and a MOS transistor bias circuit portion and having a least on output of the second integrate feedback connected to the bias circuit portion of the same integrator through a feedback block. With regards to claims 4, 5, 9 11-15 and 21, the prior art of record does not disclose or fairly teach the outputs of the first integrator being connected to the inputs of the second integrator and being coupled to ground by respective diodes. With regard to claim 7, the prior art of record does not disclose or fairly teach using the specific equation recited in claim 7 in order to emulate a capacitor. With regards to claims 16 and 17, the prior art of record does not disclose or fairly teach receiving a differential input signal from a disk drive read channel at a simulated non linear inductor circuit having bipolar transistors.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly E. Glenn whose telephone number is (571)-272-1761. The examiner can normally be reached on Monday-Friday 7:30 to 4:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimberly E Glenn

Examiner

Art Unit 2817

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Robert Pascal

Supervisory Patent Examiner
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